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BOX RCE
Attorney Docket 8041-1011
PATENT

IN THE U.S. PATENT AND TRADEMARK OFFICE

10/22/2

Applicant:

Koji FURUSAWA/

Confirmation No. 3216

Appl. No.:

09/939,761

Group: 2,815

Filed:

August 28, 2001

Examiner: E. Or

For:

SEMICONDUCTOR DEVICE

RECEIVED

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REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. § 1.114

BOX RCE

Assistant Commissioner for Patents Washington, DC 20231

Date: October 15, 2002

Sir:

This is a "Request for Continued Examination" under 37 C.F.R. \S 1.114, the provisions of which do <u>not</u> apply to:

- (1) A provisional application; (2) An application for a utility or plant patent filed under 35 U.S.C. 111(a) before June 8, 1995; (3) An international application filed under 35 U.S.C. §363 before June 8, 1995; (4) An application for a design patent; or (5) A patent under reexamination.
- This Request for Continued Examination is being filed prior to the earliest of:
 - (1) Payment of the issue fee, unless a petition under \$1.313 is granted; (2) Abandonment of the application; or (3) The filing of a notice of appeal to the U.S. Court of Appeals for the Federal Circuit under 35 U.S.C. § 141, or the commencement of civil action under 35 U.S.C. §§ 145 or 146, unless the appeal or civil action is terminated.
- The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.
- The enclosed document is being transmitted via facsimile.

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Submission Required under 37 C.F.R. § 1.114:

Enter as part of the present submission:

- An After Final Amendment previously filed on , under 37 C.F.R. § 1.116 but unentered, in the present application.
- Arguments in the Appeal Brief or Reply Brief previously filed on .
- A Reply Under Rule 1.111, attached hereto. Claim fee(s) are calculated as set forth below:

	TOTAL NUMBER OF CLAIMS PREVIOUSLY FILED	TOTAL NUMBER OF CLAIMS BEING FILED HEREWITH	NUMBER EXTRA	RATE_	FEE
Total Claims	15	15	0	x\$18 =	\$.00
Independent Claims	4	4	0	x\$84 =	\$.00
			TOTAL (FEE(S)	CLAIM	\$.00

- An Information Disclosure Statement (IDS) and PTO-1449 form(s) is/are attached hereto for the Examiner's consideration.
- Other: Amendment

⊠ <u>Fees</u>

The required fee under 37 C.F.R. \$ 1.17(e) as required by 37 C.F.R. \$ 1.114 when the RCE is filed, is enclosed herewith:

- ☐ \$355.00 small entity
- \boxtimes \$740.00 large entity

Appl. No. 09/939,761

	purs	applicant hereby petitions for an extension month want to 37 C.F.R. §§ 1.17 and 1.136(a). The fee has been ulated as shown below:
		NO extensions of time have been previously obtained in the prior application. Thus, a fee of \$.00 is required for the full period of the above-requested extension of time.
		An extension of one () month was previously requested and paid for on in the instant application. Thus, a fee of \$0.00 is required to obtain an () month extension.
\boxtimes	app1:	osed is a check in the amount of \$740.00 for the icable filing fee, additional claims fee, and/ornsion fees.
	Pleas \$0.00	se charge Deposit Account No. 25-0120 in the amount of D. A triplicate copy of this sheet is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. §\$1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

YOUNG & THOMPSON

Rv

Liam McDowell

Attorney for Applicants Registration No. 44,231 745 South 23rd Street Arlington, VA 22202 Telephone: 521-2297

October 15, 2002

Attachments

(REV. 09/29/2000)

Attorney Docket No. 8041-1011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Koji FURUSAWA

Serial No. 09/939,761

Filed August 28, 2001

SEMICONDUCTOR DEVICE

Confirmation No. **GROUP 2815**

Examiner Edgardo

AMENDMENT

Commissioner for Patents

Washington, D.C. 20231

Sir:

Responsive to the Official Action of July 15, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Amend the claims as follows:

(amended) A semiconductor device comprising:

a substrate;

first semiconductor chip on said substrate;

second semiconductor chip overlying said first semiconductor chip;

layer**** between wiring said first semiconductor chips, said wiri $h_{\mathcal{Q}}$ layer including a polyimide tape having a copper foil layer there in;

a plurality of bonding pads on said wiring layer, said substrate and said first and second seconductor chips; and